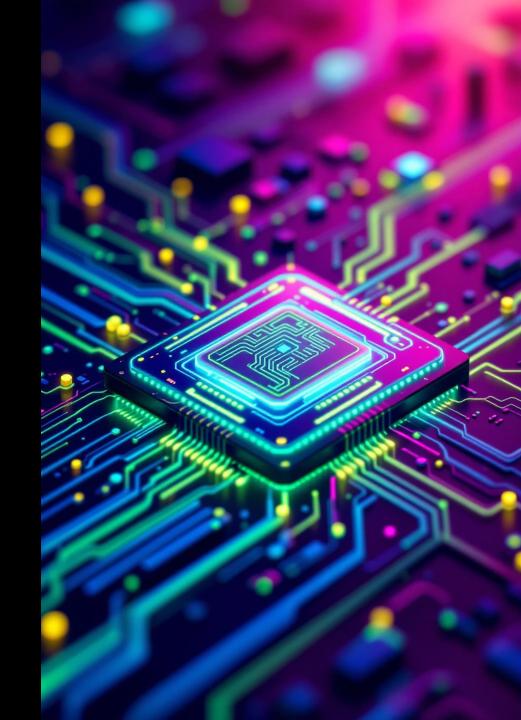


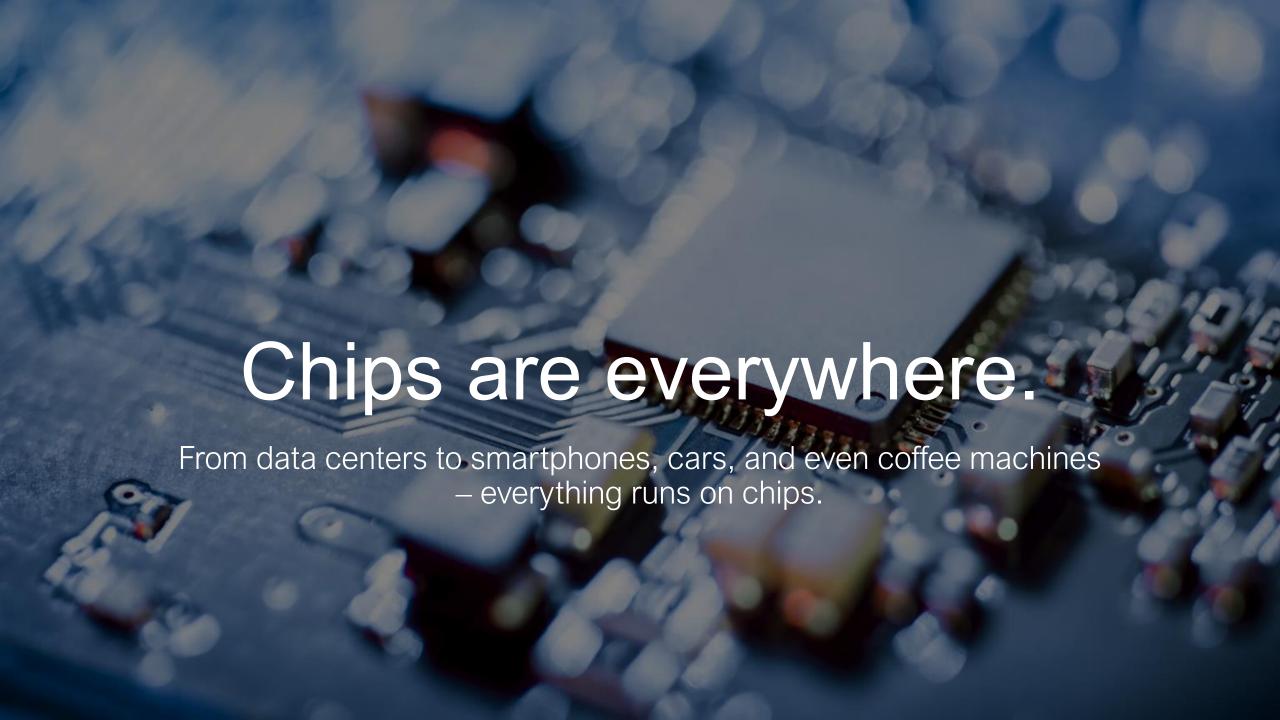
We develop hardware functions that is critical for the on-chip data communication

Our customers are Chip design companies

Founded 2024

Based on R&D since 2019





The new challenge for chip designers

Al trend: ever-growing demand for computing power



Historically

Scaling computer power was straightforward – just make the chip's components smaller and add more of them.

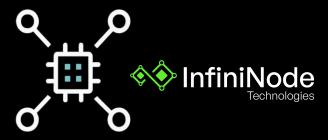
2000 transistors



Now

Chips are already packed to the limit. Components are so small and dense that simply shrinking them further no longer works.

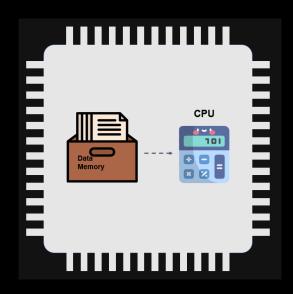
184 billion transistors

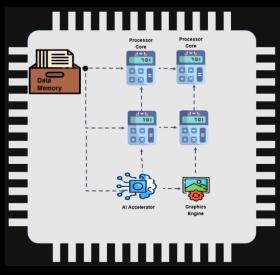


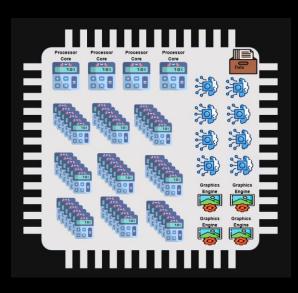
The new BIG problem

New (Complex) Architecture
On-Chip communication
Memory management

The Critical Must Have Interconnect

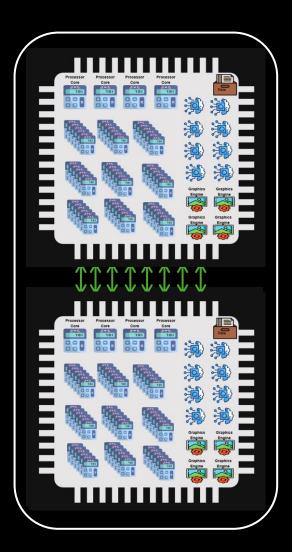


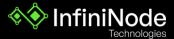




Why InfiniNode

- Scalable solution up to 128 cores
- Chiplet readiness
- Team expertise
- Market is here Al compute demand doubles until 2030





The Semiconductor Value Chain













Raw materials

and components

The fabless model

In-house chip design with outsourced manufacturing



Design software, R&D tools, and IP SYNOPSYS arm cādence **SIEMENS /**Insys Qualcomm **KEYSIGHT ##**LATTICE

Rambus





Nikon PRODUCTS 12

supplier layer Supplying both sides through all stages of chip development

The



The integrated model

Vertically integrated chip development

InfiniNode: Powering Europe's Sovereign Compute Ambitions



€43 billion EU Chips Act €100+ billion in public-private projects €2+ billion in AI infrastructure



InfiniNode's Strategic Position in Europe

Trusted IPs in EU-funded projects

Well positioned for chiplet-based SoCs



InfiniNode help chip designers meet tomorrow's demands for processing power.

We provide chip designers with the critical functions that enable seamless on-chip communication.



Premium IPs for Lower cost

Lower cost vs inhouse development & licensing from market giants



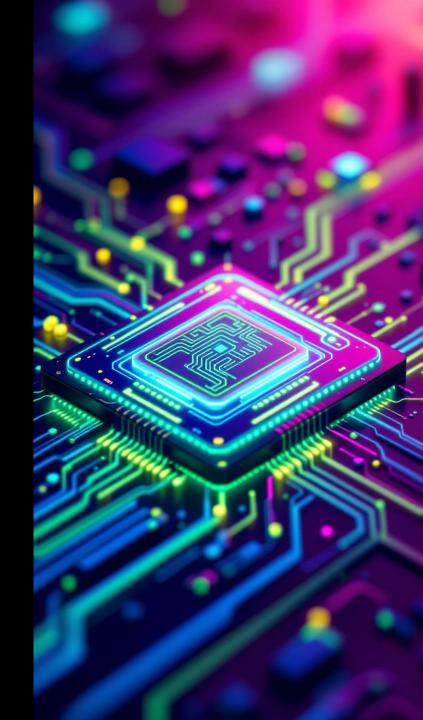
Faster to market

Quicker than developing everything in-house.

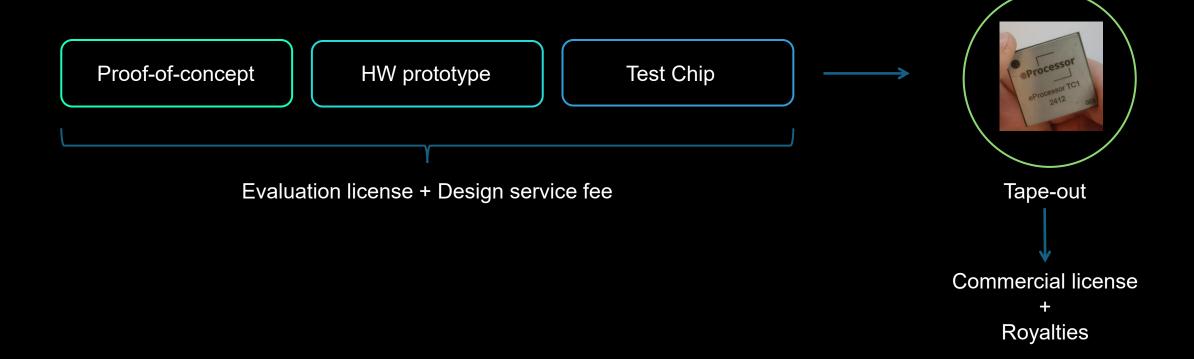


Future-ready

Scales beyond today's needs (up to 128 cores)



Business model: License + design service fee + Royalties





On-chip interconnect 2030 market outlook







Go-To-Market Strategy
Focus on AI accelerator companies

\$ 10-15 billion TAM



Customer traction

- Ongoing projects with three actors





ZeroPoint 🗩

Sold Evaluation License

LOI

LOI partnership agreement

Partnership to evaluate a combined product offering with our Cache IP and their compression IP.



CHALMERS spinoff with top academics and industry experts















CEO Patrik Millsjö

+15 yrs with int. Sales in Semiconductor & outsourcing projects

Capgemini

aLTRan

ERICSSON 🗯

Prof. loannis Sourdis

2 Decades of track record in design of interconnection networks and acceleration technologies

Internationally renowned researcher

Dr. Ahsen Ejaz

Proven track record in interconnection networks design and implementation

Extensive industrial and academic experience

Dr. Bhavishya Goel

Proven track record in cache design and implementation

Extensive industrial and academic experience

Dr. Madhavan Manivannan

Experienced in chip design and performance evaluation

Multiple publications related to cache technology

Dr. Mehrzad Nejat

Proven track record in cache design and implementation

Extensive industrial and academic experience

Prof. Per Stenström

Decades of track record in cache design

Internationally renowned researcher

2x startup founder





Preparing for Next Round Q1-26

Goal with investment:

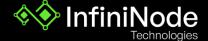
This investment accelerates us from deep-tech readiness to commercial proof. By month 18, we'll have validated our IP, signed our first customer, and built the foundation for scaling.

Investment needed: 10MSEK

Key activities:

- Core Tech demonstrator ready, validating technology with customer
- 2 new partnership project
- 2 patents filed

CEO – Patrik Millsjö <u>Patrik@infininode.com</u> +46 705 666 369



InfiniNode Technologies

Helping chip designers meet tomorrow's demands for processing power.

